Amendments to the Specification:

Please replace paragraph [0055] with the following amended paragraph:

[0055] The rotating phasor in equation 6, $e^{-i(\omega_s-\omega_{LO})t}/E_{LO}^*$, contains $(\omega_s-\omega_{LO})t-\varphi$, the phase of the signal with respect to the LO, which is not provided directly to the DSP and must be calculated by it from beat term 1 and beat term 2. Only when the estimate of $(\omega_s-\omega_{LO})t-\varphi$ is correct continuously over time (when the phase estimation algorithm is locked) may the data be recovered with a low bit error rate. After locking has occurred, the phase term wanders because of the finite linewidth of the signal and LO lasers over a time of typically many bit periods. The phase estimation algorithm must then track this phase wander. There are many types of phase estimation algorithm that can be implemented within the DSP, as described in "Digital Communications" by John G. Proakis (Proakis). If the modulation format of the incoming signal contains a pilot carrier then a digital phase locked loop (PLL) or an open loop phase estimation algorithm can be applied to (beat term 1)+i(beat term 2) directly. An example of an open loop phase estimation algorithm is taking the arctangent of the ratio (beat term 2)/(beat term 1) followed by a low pass filter function. When the signal's modulation format is such that it contains no carrier then (beat term 1)+i(beat term 2) must first be processed by a ~~single~~ <u>spectral</u> line generation function, such as a squaring function (or power law function in the case of high order PSK), or a decision directed multiplication, or in a Costas loop which combines the single line generation function with the PLL. An alternative method of estimating the phase is to make use of known sequences of symbols that are repeated in the transmitted signal every time interval τ_{seq}, but this kind of method is useful only when the frequency difference between the signal and local oscillator is small, less than $½\tau_{seq}$.

Please replace paragraph [0060] with the following amended paragraph:

[0060] FIG. 3B illustrates a simplified block diagram of a balanced quadrature sampling receiver 70 in a first alternate embodiment of the present invention. Each of the phase diverse arms is further split into two balanced arms. The contents of the

dashed box are a four branch phase diversity hybrid unit 72. To perform the subtraction of detected signals associated with balanced detection, either two differential amplifiers 74 and 76 may be used followed by ~~A/D~~ A/D converters 78 and 80, or four separate A/D converters 82, 84, 86, and 88 can be used and the balanced detection result obtained by subtraction within the DSP.

Please replace paragraph [0067] with the following amended paragraph:

[0067] Existing Methods of Polarization ~~Trackinq~~ Tracking

Please replace paragraph [0070] with the following amended paragraph:

[0070] To achieve polarization scrambling, which is described in "Polarization switching techniques for coherent optical ~~communications~~ communications" by I. M. I. Habbab and L. J. Cimini (Habbab) and Noe, an extra modulation element is included in the transmitter, which changes the SOP of the signal substantially within one symbol period. At the receiver, the coherent beat term is effectively an average of all the relative SOPs, aligned and orthogonal, during the bit period, thus avoiding persistent orthogonality. Polarization scrambling suffers from the disadvantage of utilizing an expensive scrambler element in the transmitter. In addition, the act of scrambling broadens the linewidth of the signal, which limits the density of WDM channels and makes the signal more susceptible to fiber propagation impairments.

Please replace paragraph [0071] with the following amended paragraph:

[0071] FIG. 4A is a simplified block diagram of an existing configuration 91 for polarization diversity detection. This solution is described in Noe. The signal 90 and local oscillator 92 are each divided into two paths (in addition to any splitting of paths for balanced detection or phase and quadrature detection). The splitting of the LO by a polarization splitter 94 is such that its SOP in the two paths is orthogonal (e.g., horizontal in the top path and vertical in the lower path). The SOP of the signal is the same in the two paths. There are two separate coherent receivers (photodetectors 96 and 98) in the two paths, and their outputs are summed together after demodulation of the IF, by demodulators 100 and 102. Then the summed result is passed to the decision

circuit. Within this configuration, immunity to the varying incoming signal SOP is achieved because in the situation where one path has the LO and signal SOPs orthogonal, they are aligned in the other path. The variable gain amplifiers in the two paths are used to avoid a variation of the peak-to-peak magnitude of the summed signal due to changes in the incoming signal SOP, as discussed in "Signal processing in an optical polarization diversity for 560-Mbit/s ASK heterodyne detection" by B. Enning et al. (Enning). In addition; with polarization diversity, it is possible for the incoming signal SOP to vary in a manner which does not cause the relative power aligned with the LO in the two arms to change, but it is equivalent to the phase of the signal relative to the LO changing continuously (beyond 2π) in one arm, while the phase of the signal is fixed with respect to the LO in the other arm. However, for homodyne detection, it is necessary to have zero phase difference between the signal and local oscillator (i.e., phase locking) in both arms of the polarization diverse configuration. Therefore, polarization diversity cannot be used with homodyne detection. U.S. Pat. No. 5,322,258 to ~~Tsuchima~~ Tsushima (Tsushima) disclosed using an electro-optic phase modulator in one arm of the LO to ensure that the phase is matched, but in fact electro-optic modulators provide only a limited range of phase shift, and therefore does not provide endless polarization tracking.

Please replace paragraph [0131] with the following amended paragraph:

[0131] MPI compensation can be achieved by implementing a digital filter within the DSP. As explained in Lyons, the output $y(n)$ of a general recursive digital filter is computed from the input $x(n)$ by:

$$\cancel{y(n)=\sum_{k=0}^{\infty}a_k x(n-k)+\sum_{k=0}^{\infty}b_k y(n-k)}$$

$$\underline{y(n)=\sum_{k=0}^{\infty}a_k x(n-k)+\sum_{k=1}^{\infty}b_k y(n-k)}$$